REMARKS

Claims 1, 2, 4-13, 15-21 and 23-24 are in the application. Claims 3, 14, 17-20, and 22 have been cancelled.

By this amendment, applicants have amended claims 1, 7, and 21 to more particularly set out and claim the subject matter of their invention. Cancelled claims 3, 14 and 22 support the changes to these claims.

Further, claims 2, 5, 9, 10, 23 and 24 have been amended to have proper antecedent basis in view of the amendments made to claims 1, 7 and 21, and to address the §112 second paragraph rejection.

Response to 35 U.S.C. §112 Rejection

Claims 1-6, 9-10 and 24 were rejected under 35 U.S.C. §112, second paragraph. Applicants have amended these claims to utilize the language suggested by Examiner Staicovici, and respectfully believe that these claims now meet the requirements of §112, second paragraph.

Non-Statutory Double Patenting Rejection

Claims 1-16 and 21-24 were rejected on the grounds of non-statutory obviousness-type double patenting over U.S. Patent No. 6,835,580 in view of JP 2001-230520 and U.S. Patent No. 5,766,972.

Applicants have timely filed herewith a terminal disclaimer in compliance with 37 C.F.R. 1.321, thus making this rejection moot.

Response to 35 U.S.C. §103 Rejection

Claims 1-2, 4-13, 21 and 24 were rejected under 35 U.S.C. §103(a) as being unpatentable over applicants' admitted prior art ("APA") in view of JP 2001-230520 ("Sony") and in further view of Takahashi et al., USP 5,766,972 ("Takahashi"). Applicants respectfully traverse this rejection in view of the amendments made herein and the remarks presented hereinafter.

Claim 1 calls for a method for forming a direct chip attach device comprising the steps of attaching an electronic chip to a lead frame structure, wherein the electronic chip includes a bonding pad. The method also calls for attaching a conductive bump to the bonding pad and placing the electronic chip and lead frame structure into a molding apparatus, wherein the molding apparatus has a well portion with a removable pin coupled to a first surface of the well portion. Additionally, the method calls for contacting the removable pin to the conductive bump and molding the electronic chip with an encapsulating material, wherein the removable pin masks the conductive bump to provide an opening in the encapsulating material over the conductive bump, and wherein the conductive bump is recessed within the opening. Further, the method calls for thereafter forming a barrier layer overlying the conductive bump.

Firstly, applicants respectfully submit that there is no motivation to combine the Sony reference with the APA and Takahashi. Specifically, the Sony reference addresses the injection molding of printed circuit boards, and further makes no suggestion that the process disclosed therein is relevant to the encapsulation of semiconductor devices or

more specifically to direct chip attach semiconductor devices.

Assuming arguendo that there is motivation to combine the references, the combination of references still fails to show or suggest the method now set forth in applicants' claim 1. Specifically, none of the relied upon references either singularly or in combination show or suggest placing an electronic chip attached to a leadframe structure into molding apparatus having a removable pin coupled to a first surface of the well portion. In the Sony reference, there is no teaching or suggestion that the pins are removable. Applicants further submit that this is not a minor difference, because a removable pin greatly increases the flexibility of the manufacturing process as is more particularly described in paragraph [0025] of their specification.

In addition, neither the Sony reference nor the Takahashi reference show or suggest forming an opening where the conductive bump is recessed within the opening. The Sony reference is in fact silent on this element, and the Takahashi reference specifically states that his conductive bump 30a and the surface of the molding resin 5 are in the same plane (see Column 9, lines 41-48). Applicants further submit that this is not a minor difference either, because applicants' recessed opening provides, among other things, enhanced alignment for further assembly structures such as solder balls, which is further described in paragraph [0021] of their specification.

Further, neither the Sony reference nor the Takahashi reference show or suggest thereafter forming a barrier layer overlying the conductive bump. Thus, for at least these

reasons, applicants respectfully submit that claim 1 is allowable over the cited references.

Claim 2 depends from claim 1 and is believed allowable for at least the same reasons as claim 1.

Claim 4 depends from claim 1 and is believed allowable for at least the same reasons as claim 1.

Claims 5 depends from claim 1 and further calls for the step of placing the electronic chip and the lead frame structure into the molding apparatus to include placing the electronic chip and the lead frame structure into the molding apparatus, wherein the removable pin has a flat upper surface and rounded upper edges. Claims 5 is believed allowable for the same reasons as claim 1. Additionally, applicants respectfully submit that claim 5 is allowable because none of the relied upon references show or suggest a removable pin having a flat upper surface and rounded upper edges. Applicants further submit that this is not a minor difference because this step provides for an enhanced alignment feature in the resultant structure for attaching a next level of assembly such as solder balls as described in paragraph [0021].

Claim 6 depends from claim 1 and is believed allowable for at least the same reasons as claim 1.

Claim 7 calls for a process for forming a flip-chip device comprising the steps of placing a sub-assembly into a mold apparatus having a cavity, wherein the sub-assembly comprises an electronic chip attached to a support substrate, and wherein the electronic chip has a first conductive stud coupled to the electronic chip. The process also calls for contacting the first conductive stud with a first blocking device in the cavity. The process further calls for injecting an encapsulating material into the

cavity to encapsulate the electronic chip, wherein the first blocking device masks the first conductive stud to form an opening in the flip-chip device, wherein the opening comprises a chamfered edge, and wherein the first conductive stud is recessed within the opening. Still further, the process calls for forming a barrier layer overlying the first conductive stud.

Firstly, applicants respectfully submit that there is no motivation to combine the Sony reference with the APA and Takahashi. Specifically, the Sony reference addresses the injection molding of printed circuit boards, and further makes no suggestion that the process disclosed therein is relevant to the encapsulation of semiconductor devices or more specifically to direct chip attach semiconductor devices.

Assuming arguendo that there is motivation to combine the references, the combination of references still fails to show or suggest the process now set forth in applicants' claim 7. Specifically, neither the Sony reference nor the Takahashi reference show or suggest a process wherein the first blocking device masks the first conductive stud to form an opening in the flip-chip device, wherein the opening comprises a chamfered edge, and wherein the first conductive stud is recessed within the opening after the encapsulation step. The Sony reference is in fact silent on this element, and the Takahashi reference specifically states that his conductive bump 30a and the surface of the molding resin 5 are in the same plane (see Column 9, lines 41-48). Applicants further submit that this is not a minor difference because applicants' recessed opening provides, among other things, enhanced alignment for further assembly structures such as solder balls, which is further described

in paragraph [0021] of their specification. Further, none of the relied upon references show or suggest forming a barrier layer overlying the conductive stud. Thus, for at least this reason, applicants respectfully submit that claim 7 is allowable over the cited references.

Claim 8 depends from claim 7 and is believed allowable for at least the same reasons as claim 7.

Claim 9 depends from claim 7 and further calls for the step of contacting the first conductive stud to include contacting the first conductive stud with a removable pin coupled to the mold apparatus. Claim 9 is believed allowable for the same reasons as claim 7. Additionally, applicants respectfully submit that claim 9 is allowable because none of the relied upon references show or suggest a contacting the first conductive stud with a removable pin coupled to the mold apparatus.

Claims 10 depends from claim 9 and further calls for the step of contacting to include contacting the first conductive stud with a removable pin having a flat upper surface and rounded upper edges to form the chamfered opening. Claim 10 is believed allowable for the same reasons as claims 9 and 7. Additionally, applicants respectfully submit that claim 10 is allowable over the cited references because they do not show or suggest contacting the first conductive stud with a removable pin having a flat upper surface and rounded upper edges to form the chamfered opening.

Claim 11 depends from claim 7 and further calls for the step of placing the sub-assembly to include placing a sub-assembly having an electronic chip attached to a support substrate, wherein the support substrate includes a flag. Applicants respectfully believe that claim 11 is allowable

for the same reasons as claim 7. Additionally, applicants respectfully submit that none of the relied upon references show or suggest placing a sub-assembly having an electronic chip attached to a support substrate, wherein the support substrate includes a flag. Applicants respectfully disagree with the Examiner's assessment that flags are known, particularly when taken in the context of the other express steps set forth in applicants' claim 7. More particularly, applicants respectfully submit that the prior art does not teach or suggest the use of a flag in combination with contacting a first conductive slug with the first blocking device. Thus, applicants respectfully believe that claim 11 is allowable for this additional reason.

Claim 12 depends from claim 11 and is believed allowable for at least the same reasons as claims 11 and 7.

Claim 13 depends from claim 7 and is believed allowable for at least the same reasons as claim 7.

Claim 15 depends from claim 7 and further calls for the step of placing the sub-assembly to include placing a sub-assembly having an electronic chip attached to a support substrate, wherein the support substrate includes a flag with a second conductive stud attached to the flag. Applicants respectfully believe that claim 15 is allowable for the same reasons as claim 7. Additionally, applicants respectfully submit that claim 15 is allowable over the cited references because of none of the references show or suggest a step of placing a sub-assembly having an electronic chip attached to a support substrate, wherein the support substrate includes a flag with a second conductive stud attached to the flag.

Claim 16 depends from claim 15 and further calls for contacting the second conductive stud with a second blocking

device in the cavity. Applicants respectfully believe that claim 16 is allowable for the same reasons as claim 15 and 7. Additionally, applicants respectfully submit that claim 16 is allowable because none of the relied upon references show or suggest contacting the second conductive stud with a second blocking device in the cavity.

New claim 21 calls for a method for forming a semiconductor device comprising the steps of placing a sub-assembly into a mold apparatus having a cavity, wherein the sub-assembly comprises an electronic chip attached to a support substrate, and wherein the electronic chip has a first conductive stud coupled thereto, and wherein the support substrate further includes a flag having a second stud coupled thereto. The method also calls for contacting the first conductive stud with a first blocking device in the cavity and contacting the second conductive stud with a second blocking device in the cavity. Additionally, the method calls for injecting an encapsulating material into the cavity to encapsulate the electronic chip and the flag, wherein the first blocking device masks the first conductive stud to form a first opening having a chamfered edge in the encapsulating material and overlying the first conductive stud, and wherein the second blocking device masks the second conductive stud to form a second opening having a chamfered edge in the encapsulating material and overlying the second conductive stud. In addition, the method calls for forming a barrier layer overlying the first and second conductive studs. Further, the method calls for attaching a first solder ball to the first conductive stud through the first opening, wherein the chamfered edge of the first opening is configured to enhance alignment of the first solder ball in the first opening and attaching a second

solder ball to the second conductive stud through the second opening, wherein the chamfered edge of the second opening is configured to enhance alignment of the second solder in the second opening.

Firstly, applicants respectfully submit that there is no motivation to combine the Sony reference with the APA and Takahashi. Specifically, the Sony reference addresses the injection molding of printed circuit boards, and further makes no suggestion that the process disclosed therein is relevant to the encapsulation of semiconductor devices or more specifically to direct chip attach semiconductor devices.

Assuming arguendo that there is motivation to combine the references, the combination of references still fails to show or suggest process now set forth in applicants' claim 21. Specifically, none of the relied upon references either singularly or in combination show or suggest injecting an encapsulating material into the cavity to encapsulate the electronic chip and the flag, wherein the first blocking device masks the first conductive stud to form a first opening having a chamfered edge in the encapsulating layer and overlying the first conductive stud, and wherein the second blocking device masks the second conductive stud to form a second opening having a chamfered edge and overlying the second conductive stud. The Sony reference is in fact silent on this element, and the Takahashi reference specifically states that his conductive bump 30a and the surface of the molding resin 5 are in the same plane (see Column 9, lines 41-48) so there is no edge at all.

Further, neither reference shows or suggests attaching a first solder ball to the first conductive stud through the first opening, wherein the chamfered edge of the first

opening is configured to enhance alignment of the first solder ball in the first opening and attaching a second solder ball to the second conductive stud through the second opening, wherein the chamfered edge of the second opening is configured to enhance alignment of the second solder in the second opening. Moreover, none of the relied upon references show or suggest forming a barrier layer overlying the first and second conductive studs. Thus, for at least these reasons, applicants respectfully submit that claim 21 is allowable over the cited references.

Claim 23 depends from claim 21 and is believed allowable for at least the same reasons as claim 21.

Claim 24 depends from claim 21 and further calls for the step of contacting the first conductive stud with the first blocking device to include contacting the first conductive stud with a removable pin having a flat contact surface and rounded edges adjacent the flat contact surface. Applicants respectfully believe that claim 24 is allowable for the same reasons as claim 21. Additionally, applicants respectfully submit that claim 24 is allowable because none of the relied upon references show or suggest a step of contacting a first conductive stud with a removable pin having a flat contact surface and rounded edges adjacent the flat contact surface.

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In view of all of the above, it is believed that the application is in condition for allowance, which action is earnestly solicited.

Applicants' undersigned representative respectfully requests that Examiner Staicovici contact him directly if there are any further issues to discuss in order to move the case this to allowance.

The Commissioner is hereby authorized to charge Deposit Account No. 501086 in the amount of $130.00 due for the Statutory Disclaimer Fee set forth in 37 CFR 1.20(d).

Respectfully submitted,

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